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[2885/21]

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Inventors	:	Martin VORBACH et al.
Serial No.	:	09/335,974
Filing Date	:	June 18, 1999
For	:	I/O AND MEMORY BUS SYSTEM FOR DFPS AND UNITS WITH TWO-OR MULTI-DIMENSIONAL PROGRAMMABLE CELL ARCHITECTURES
Group Art Unit	:	2781
Examiner	:	Gopal RAY

I hereby certify that this correspondence is being deposited with the United States Postal Service as first class mail in an envelope addressed to: Assistant Commissioner for Patents and Trademarks, Washington, D.C. 20231, on

Date 9 Nov 00 Atty's Reg. # 38,099

Atty's Signature

MICHELLE M. CARNIAUX
KENYON & KENYON

Assistant Commissioner for Patents
Washington, D.C. 20231

AMENDMENT

SIR:

This paper addresses the Office Action dated May 10, 2000. Initially, please amend the above-identified application as follows:

IN THE DRAWINGS:

Please amend the drawings as indicated in the attached red-marked sheets.

IN THE SPECIFICATION:

Please amend the specification as follows:

On page 1, line 2, after "Application", insert --No.--.

On page 1, line 8, delete "DE".

On page 3, line 6, replace "4" with --4a--.

On page 3, before line 10, insert:

--Figure 4b shows an example of line bundling in FPGAs according to another example

A1